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Few-layer $SnSe_2$ transistors with high on/off ratios

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We report few-layer $SnSe_2$ field effect transistors (FETs) with high current on/off ratios. By trying different gate configurations, 300 nm SiO_2 and 70 nm HfO_2 as back gate only and 70 nm HfO_2 as back gate combined with a top capping layer of polymer electrolyte, few-layer $SnSe_2$ FET with a current on/off ratio of 10^4 can be obtained. This provides a reliable solution for electrically modulating quasi-two-dimensional materials with high electron density (over $10^{13}\,cm^{-2}$) for field-effect transistor applications. © *2016 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4941394]

Graphene's success has triggered extensive research on isolation, characterization, and device applications of two-dimensional (2D) layered materials.[1] The successful isolation and synthesis of transition-metal dichalcogenide (TMD) atomic layers such as MoS_2 boosted the research on exploration of fundamentally interesting physical phenomena and technological applications in electronics and optoelectronics benefiting from their sizeable and thickness-dependent bandgaps, which are not present in graphene.[2,3] In TMDs, the *d* electrons are the main source to form lower valence band maxima, inducing a band transition from indirect to direct bandgap when reduced to single atomic layer.[4] Consequently, strong photoluminescence properties are present in single-layer TMDs.[2]

Recently, the demonstration of few-layer SnS_2 for applications in transistors,[5] logic circuits, and photodetectors[6] extends this system to dichalcogenides of metals from the main group in the periodic table of the elements. Compared to TMDs, no *d* electrons are involved in the bonding configuration of these metal dichalcogenides. As a result, new phenomena emerge. For example, the bandgap gets smaller for SnS_2 when reducing the thickness from bulk to monolayer, which is contrary to that of TMDs.[7] As a close relative, few-layered $SnSe_2$ with similar band structure has been rarely investigated.[8] Previous attempts on $SnSe_2$ field effect transistors (FETs) indicated that the current cannot be completely turned off due to the high electron density in $SnSe_2$ layers ($10^{18}\,cm^{-3}$ in bulk $SnSe_2$,[9] compared with $\sim 10^{16}\,cm^{-3}$ in MoS_2[10] and $\sim 10^{15}\,cm^{-3}$ in black phosphorus[11]). Therefore, how to effectively modulate the transport of carriers remains a challenge for FET applications of such systems. Pan *et al.* have investigated the effect of selenium substitution for sulfur in 2D SnS_2 with thickness in the range of 11–35 nm.[12] When sulfur is completely replaced with selenium, $SnSe_2$ transistors cannot be turned off. This feature was also confirmed by Su *et al.*, in whose devices the thickness of $SnSe_2$ is about 84 nm.[13] The main challenge to modulate $SnSe_2$ transistors comes from the high electron concentration in $SnSe_2$ and the difficulty in reducing the thickness of flakes.

In this study, we investigate FETs based on mechanically exfoliated few-layered $SnSe_2$ flakes. We found that, when 300 nm SiO_2 or 70 nm HfO_2 on a p^{++} Si substrate are used as back-gate dielectrics, the $SnSe_2$ FETs cannot be turned off. On the other hand, a combination of 70 nm HfO_2 as back gate with a top capping layer of polymer electrolyte, the $SnSe_2$ FETs show a high current on/off ratio over 10^4. Our findings demonstrate a reliable way to electrically modulate the 2D materials with high carrier density, which is promising for extending such systems to electronic device applications.

At first, few-layered $SnSe_2$ flakes are mechanically exfoliated onto a p^{++} Si substrate covered with 300 nm SiO_2 using a Scotch tape. Compared with that of MoS_2, the contrast of $SnSe_2$ flakes is much weaker. Figure 1(a) shows an optical micrograph of a typical exfoliated $SnSe_2$ flake. The thinnest part of the flake with a thickness of 3.7 nm is almost invisible when illuminated with white light. Due to this difficulty, we have never obtained or observed monolayer $SnSe_2$. X-ray diffraction (XRD) characterization indicates that the $SnSe_2$ crystal can be indexed as CdI_2-type layered structure (JCPDS No. 89-2939), shown in Figure 1(b). The inter-plane distance along the ⟨001⟩ direction is 6.14 Å.

In previous studies, a thickness-dependent Raman spectrum has been frequently observed in 2D TMDs materials, where the out-of-plane A_{1g} mode shows a blue shift with increasing thickness due to the stiffening of the out-of-plane phonons; on the other hand, the in-plane degenerate E_g mode shows a red shift upon the addition of extra layers due to the relaxation of in-plane bonding.[14] However, for $SnSe_2$ flakes with different thicknesses, the Raman spectra of the out-of-plane A_{1g} mode at $187\,cm^{-1}$ and in-plane E_g mode at $112\,cm^{-1}$ do not show any thickness-dependent features, as shown in Figure 1(d). Similar to MoS_2, the thickness-dependent feature disappears when it is beyond five layers.[14] In fact, there are two kinds of CdI_2-type stacking orders in $SnSe_2$ crystals, 1 T and 6Hb polytypes.[15,16] Both of their out-of-plane A_{1g} modes are located near $185\,cm^{-1}$ and in-plane

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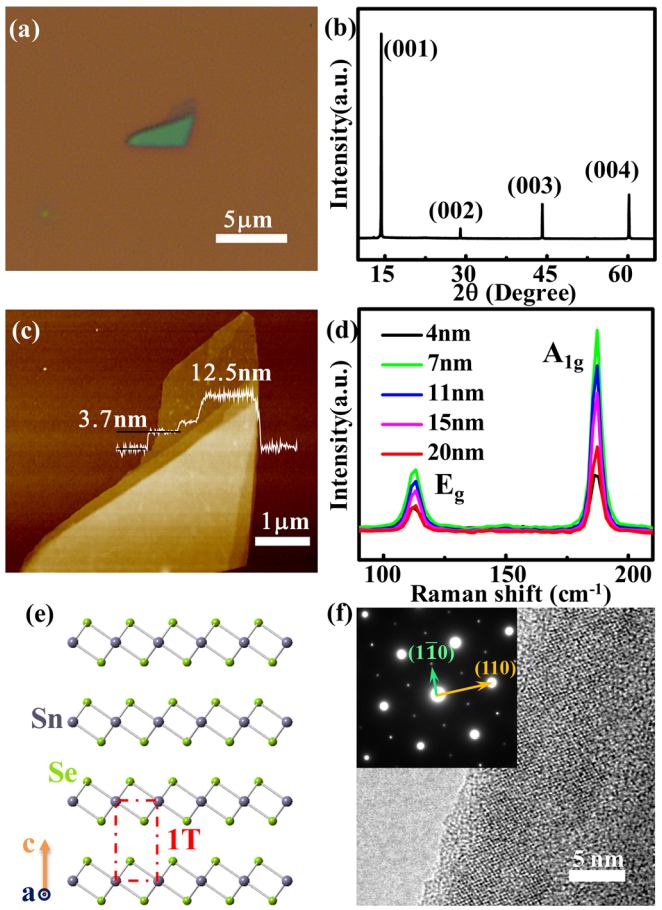

FIG. 1. (a) Optical micrograph and (c) atomic force microscopy (AFM) image of a $SnSe_2$ flake. (b) The XRD pattern of the bulk $SnSe_2$ crystal. (d) Raman spectra of $SnSe_2$ with different thickness. (e) Atomic stack schematics of 1 T $SnSe_2$ projected along [100] direction. (f) HRTEM image of $SnSe_2$. Inset: Selected-area electron diffraction (SAED) of $SnSe_2$ along [001] zone axis. Yellow arrow represents crystal plane (110) with inter-planar spacing of 1.9 Å, and green arrow represents crystal plane (1$\bar{1}$0) with inter-planar spacing of 3.3 Å.

E_g modes located around 110 cm^{-1}, making it quite difficult to identify the special polytype just based on the Raman or XRD pattern. Selected-area electron diffraction (SAED) and transmission electron microscopy (TEM) of $SnSe_2$ crystal are shown in Figure 1(f), where diffraction spots from {110} and {1$\bar{1}$0} planes are present. Because the diffraction spots from crystal planes {1$\bar{1}$0} are forbidden in 6Hb type $SnSe_2$, the structure of $SnSe_2$ in our study can be identified as 1 T polytype.

$SnSe_2$ FETs are fabricated by a standard electron-beam lithography technique followed by deposition of Cr/Au (6/60 nm) in sequence as contact electrodes. All electrical characterizations are performed at room temperature in a vacuum chamber with pressure lower than 10^{-5} Torr, and the electrical properties are measured using a Keithley 4200-SCS system. A representative optical photograph of a $SnSe_2$ FET is shown in Figure 2(a). To evaluate the contact resistance, both two- and four-probe measurements are performed. As shown in Figure 2(b), a good linear relationship between the current and bias voltage indicates a good Ohmic contact between Cr/Au electrodes and the interface of $SnSe_2$. Moreover, the coincidence between two- and four-probe measurements suggests a low contact resistance.

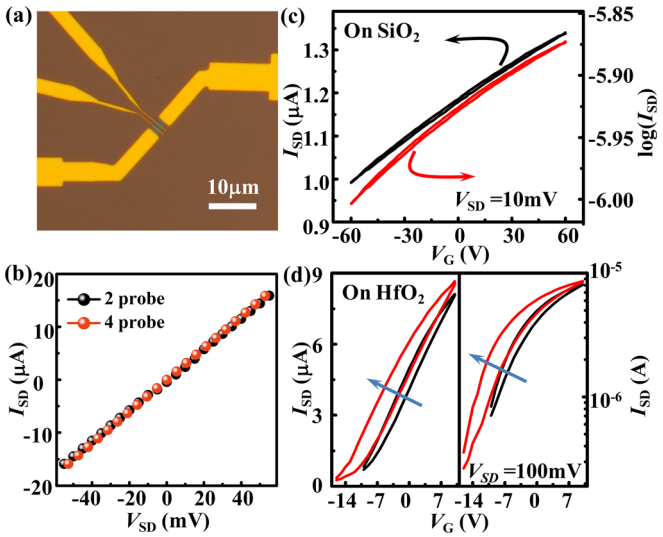

FIG. 2. (a) Optical microscopy image of a few-layer $SnSe_2$ transistor. (b) Four- and two-probe *I-V* curves of a few-layer $SnSe_2$ transistor.(c) Transfer characteristic of a few-layer $SnSe_2$ with 300 nm SiO_2 as the gate insulator. (d) Transfer characteristics of a few-layer $SnSe_2$ with 70 nm HfO_2 as the gate insulator, which move backward with the increase in sweeping scope.

Figure 2(c) presents the transfer curve of the $SnSe_2$ FET based on 300 nm SiO_2 as dielectric insulator. When we sweep the back-gate voltage V_G from −60 V to +60 V and back sweep it from +60 V to −60 V, the few-layered $SnSe_2$ exhibits an n-type conduction behavior with an electron mobility about 41 $cm^2 V^{-1} s^{-1}$, extracted from $\mu = [L/(WC_iV_{SD})] \times [dI_{SD}/dV_G]$, where L and W are channel length and width, respectively, and C_i is the capacitance per unit area of back gate insulator. The obtained electron mobility (41 $cm^2 V^{-1} s^{-1}$) in our device is almost five times higher than a previous report (8.6 $cm^2 V^{-1} s^{-1}$).[13] However, the current cannot be completely turned off even by increasing the gate voltage to −100 V. No apparent hysteresis behavior is present in the transfer curves, indicating a fully capacitive coupling and low interface defect density between the interface of $SnSe_2$ and SiO_2.

We can derive the threshold voltage V_T by extrapolation of the linear part of the transfer curve according to the equation: $I_{SD} = (WC_iV_{SD}/L) \times (V_G - V_T)$. The V_T of the device on SiO_2 is about −305 V. We can calculate the area density of electrons in the $SnSe_2$ flake by $Q = C_{SiO_2} \cdot V_T/e$, about 2.2×10^{13} cm^{-2}, where $C_{SiO_2} = 11.5$ nF cm^{-2}. It is too high to modulate with 300 nm SiO_2 as dielectric medium. To deplete the excess electrons in $SnSe_2$, we further adopt 70 nm HfO_2 as the back gate insulator. The HfO_2 is deposited onto p^{++} Si substrate by atomic layer deposition (ALD). As shown in Figure 2(d), the current on/off ratio is just beyond 10^1, even though the dielectric constant of HfO_2 (25) is 6 times higher than that of SiO_2 (3.9).[17] If we consider the $SnSe_2$ channel as 2D electron gas with area carrier density 2.2×10^{13} cm^{-2}, the threshold voltage is determined as −11.1 V by $V_T = eQ/C_{HfO_2}$ ($C_{HfO_2} = 316$ nF cm^{-2}). From the transfer curve in Figure 2(d), we can obtain the threshold voltage to be between −12.5 V and −10.7 V, which is consistent with the above assumption. However, when sweeping V_G from −16 V to 10 V, unexpectedly, the device does not turn off at −11 V.

Therefore, it is unreasonable to simply consider the electron distribution in the $SnSe_2$ flake as 2D electron gas. There

should be electrical potential difference along the vertical direction. According to semiconductor theory, if we want to deplete the excess electrons in the semiconductor, for the metal-insulator-semiconductor (MIS) structure, the thickness of the channel materials should be thinner than its maximum depletion width W_{Dm}, which is determined as[18]

$$W_{\mathrm{Dm}} \approx \left(\frac{2\varepsilon_r \varepsilon_0 \psi_{inv}}{eN_{\mathrm{D}}}\right)^{1/2}, \quad (1)$$

where ψ_{inv} is the surface potential when strong inversion occurs, N_{D} is the donor impurity concentration, ε_0 and ε_{r} represent vacuum and relative permittivity, respectively. For $SnSe_2$, because of the shallow donor energy level, which is less than 25 meV below the conduction band,[12,13] ψ_{inv} equals to the band gap (about 1 V) and N_{D} is equal to the electron density of $SnSe_2$ at room temperature, about $2.2 \times 10^{19}\,\mathrm{cm}^{-3}$ (thickness ~10 nm). The permittivity of $SnSe_2$ along the c axis, ε_{r}, is about 10.[19] Therefore, W_{Dm} of $SnSe_2$ is about 7 nm, which is smaller than the thickness of the flake. Naturally, there is no way to deplete the electrons only by the back gate modulation, regardless of how large the capacitance of the gate insulator is.

A natural way to modulate the transport of carriers in FETs is to apply a top gate using high-*k* dielectrics when the modulation of the back gate is not so effective. Therefore, we introduced a top gate to control the transporting electrons on the top surface of the $SnSe_2$ device. A high-*k* top gate dielectric is fabricated by atomic layer deposition of HfO_2. However, the $SnSe_2$ cannot survive under the "harsh" deposition conditions. Even when we lower the deposition temperature to 150 °C, the conductivity of the $SnSe_2$ still increases at least two orders of magnitude after the deposition. Another widely used technique in tuning the transport of carriers in FETs is the use of an electrochemical gate (including ionic liquid and ion gel). It is much more effective than back gate (SiO_2) and polar-dielectric-based top gate (HfO_2, Al_2O_3, etc.), due to the formation of ultra-thin (~1 nm) double layer of ions, compared to that of back gate (~300 nm) and polar-dielectric-based top gate (>5 nm).[20,21]

Here, we further adopt ionic polymer electrolyte as the top capping material in combination with 70 nm HfO_2 on p^{++} Si substrate as back gate. The polymer electrolyte is applied by spin coating with filtered (pore size 500 nm) anhydrous methanol solution of polyethylene oxide (PEO) containing 20 wt. % $LiClO_4$.[22] Then, it is annealed at 100 °C for half an hour in vacuum (50 Pa) to evaporate the solvents and solidify the electrolyte. A schematic diagram of such device is presented in Figure 3(a). Figure 3(c) gives the representative transfer curve of the $SnSe_2$ FET under the modulation of ionic polymer electrolyte as top gate (iGate). Similar to the result of back gate in Figure 2(d), the current on/off ratio is about 1, and the device is not turned off completely by the iGate modulation, in spite of the high capacitance of the polymer electrolyte (above $1\,\mu\mathrm{F\,cm}^{-2}$).[23] However, with the covered polymer electrolyte, the current on/off ratio of a $SnSe_2$ transistor increases from 10^1 to 10^4 using only back gate modulation, as shown in Figure 3(d). The sweeping rate of the voltage is 10 mV/s. If we increase the sweeping rate to 100 mV/s, the high on/off ratio also

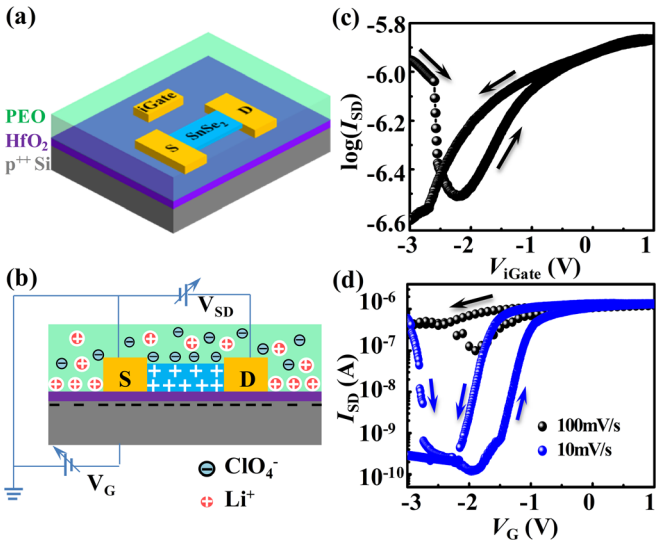

FIG. 3. (a) Schematic diagram of the geometry of $SnSe_2$ transistor covered with polymer electrolyte using 70 nm $HfO_2/p^{++}Si$ as back gate. (b) Schematic of charge accumulation by the EDL formed at the interfaces of PEO with HfO_2 and the top surface of $SnSe_2$ during gate bias sweeping. (c) Transfer characteristic of polymer electrolyte top gated $SnSe_2$ transistor. (d) Transfer characteristics of a 70 nm HfO_2 back gated $SnSe_2$ covered with polymer electrolyte measured at different sweeping rates. The iGate is disconnected.

disappears, indicating that there is ionic migration during the turn-off process.

Since there is only a back gate voltage bias applied during the measurement in Figure 3(d), what role of the capping polymer electrolyte plays in tuning the transport of carriers in $SnSe_2$ FET remains a question. The leakage current between iGate and back gate is below 10^{-10}A, suggesting no short circuit occurs. A simple model considering the series capacitance of the HfO_2 insulator and the polymer electrolyte is schematically shown in Figure 3(b). When the back gate is biased, an electrical double layer (EDL) is formed on the surface of HfO_2 near the device, which actually functions same as the iGate and induces the formation of an EDL with opposite charged inner Helmholtz plane on the top surface of $SnSe_2$ flakes. When the negative back gate voltage is applied, Li^+ ions gather on the HfO_2 surface near the flake and ClO_4^- assembles on the top surface of $SnSe_2$ flake, which deplete the electrons existing on the top surface of $SnSe_2$ and the immobile ionized donors with positive charges are remained. With the help of the polymer electrolyte, the maximum thickness of $SnSe_2$ flakes that can be modulated by the field-effect configuration increase from 7 nm to 14 nm, which covers the thickness scope of the flakes we used.

Additionally, when we increase the back gate voltage over 1 V, the current I_{SD} increases further and a turning point appears near 1.5 V, as shown in Figure 4(a). However, during the backward sweeping, I_{SD} does not decrease continuously but with steps. After the sweeping loop, the conductivity decreases three orders of magnitude. Repeating such a loop finally results in the death of the device. In Figure 4(b), Raman spectra are recorded both before and after the large positive gate bias. After the measurement, the peaks of vibration modes E_g and A_{1g} almost disappear, revealing an

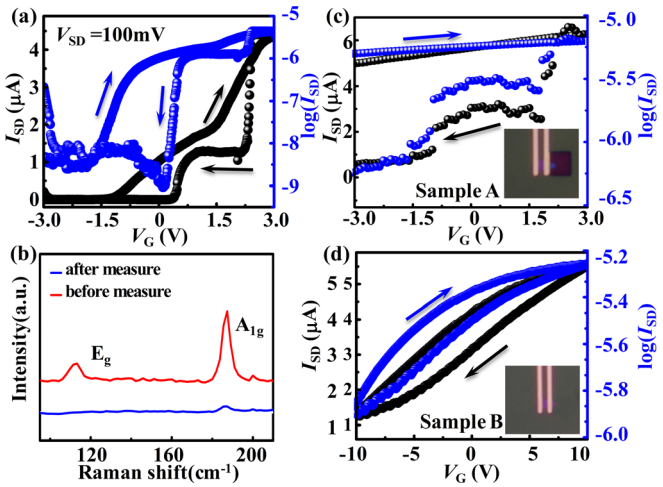

FIG. 4. (a) Transfer characteristic of 70 nm HfO_2 $SnSe_2$ cover with polymer electrolyte when gate bias sweeping from −3 V to 3 V. (b) Raman spectra of the device in (a) before and after the transfer characteristic measurement. (c) Transfer characteristic of device partly protected with PMMA, with active area is covered by PMMA and a corner is exposed to polymer electrolyte, named sample A. (d) Transfer characteristic of device fully covered by PMMA, labeled as sample B.

irreversible structural transition has occurred in the $SnSe_2$ flake. One possible origin of this transition is that Li^+ ions intercalate into the interlayer of $SnSe_2$ at large positive gate bias. To confirm this, we conducted the following control experiments.[24] In Figure 4(c), the active area of the sample A is covered by a layer of poly(methyl methacrylate) (PMMA) (300 nm) with the side corner exposed to the polymer electrolyte. The control sample B is fully protected by PMMA, as shown in Figure 4(d). Similar to the device with active area fully exposed to the polymer electrolyte, sample A also shows a stepped drop when the gate bias decreases from 3 V, indicating the diffusion of Li^+ ions happens when the gate bias reaches 3 V. Therefore, the degradation process is directly related to the Li^+ intercalation. Although the Li^+-ion intercalation can be sustained with a large positive gate bias, it becomes unstable when the gate bias decreases. Different from the TaS_2 flakes, the Li^+ ions cannot de-intercalate from the $SnSe_2$ flakes reversibly. When Li^+ ions de-intercalate, the structure of $SnSe_2$ flakes is destroyed. This causes the conductivity to decrease step by step. In lithium-ion batteries based on $SnSe_2$ as anode material, the discharge performance also degrades after several charge-discharge cycles, which implies the instability of $SnSe_2$ during the Li^+ intercalation.[25,26]

In conclusion, different gate configurations, 300 nm SiO_2, 70 nm HfO_2, and 70 nm HfO_2 combined with a polymer electrolyte, are used to modulate the transport behavior of few-layered $SnSe_2$ FETs. The current on/off ratio can be improved to 10^4 by using 70 nm HfO_2 as back-gate dielectric in combination with a layer of polymer electrolyte. Our results demonstrate a reliable way to modulate other quasi-2D systems with electron density over 10^{13} cm^{-2} and thickness about 10 nm.

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