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Insulating SiO_2 under Centimeter-Scale, Single-Crystal Graphene Enables Electronic-Device Fabrication

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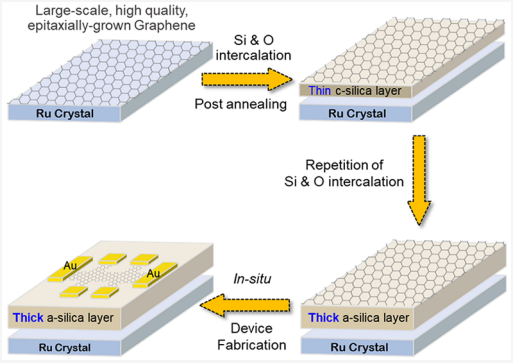
ABSTRACT: Graphene on SiO_2 enables fabrication of Si-technology-compatible devices, but a transfer of these devices from other substrates and direct growth have severe limitations due to a relatively small grain size or device-contamination. Here, we show an efficient, transfer-free way to integrate centimeter-scale, single-crystal graphene, of a quality suitable for electronic devices, on an insulating SiO_2 film. Starting with single-crystal graphene grown epitaxially on Ru(0001), a SiO_2 film is grown under the graphene by stepwise intercalation of silicon and oxygen. Thin (∼1 nm) crystalline or thicker (∼2 nm) amorphous SiO_2 has been produced. The insulating nature of the thick amorphous SiO_2 is verified by transport measurements. The device-quality of the corresponding graphene was confirmed by the observation of Shubnikov-de Haas oscillations, an integer quantum Hall effect, and a weak antilocalization effect within *in situ* fabricated Hall bar devices. This work provides a reliable platform for applications of large-scale, high-quality graphene in electronics.



KEYWORDS: *graphene, centimeter-scale, insulating SiO_2, intercalation, in situ device fabrication*

INTRODUCTION

Graphene, a two-dimensional (2D) honeycomb-structured carbon sheet, offers unprecedented prospects of solving fundamental physical problems and fabricating high-performance devices at the atomic limit.[1−10] For practical applications in future nano/quantum devices, there are crucially three conditions that must be met: (1) large-scale, at least larger than millimeter-scale, fabrication to be suitable for integration of devices, (2) atomic control of defects to guarantee the device performance, and after these two conditions are met (3) the graphene on an insulating or semiconductor layer, most importantly on Si and SiO_2, for being compatible with Si technology. To address these challenges, there are mainly three techniques that have been developed in the past decades, namely, the peeling-off technique from bulk graphite,[1,11,12] direct growth on dielectric substrates,[13−15] and epitaxial growth on metal substrates and transfer onto dielectrics.[16,17] However, using the first two techniques, the resulting graphene generally suffers from small grain size and/or low carrier mobility.[11−15] The third technique can provide large-area high-quality graphene by epitaxial growth,[17−22] especially on metal crystals,[18−20] but cannot avoid the problems accompanying the complex transfer process, such as possible interfacial contamination and quality degradation.[16,17]

Intercalation of Si between epitaxial graphene and metal substrates[23,24] has been shown to be the best way to replace the transfer technique and maintain a graphene sheet of large scale and high quality. This transfer-free technique can avoid quality degradation and possible interfacial contamination and has been used to successfully fabricate large-scale and high-quality graphene on Si monolayer/bilayer.[23] The intercalation mechanism is by now well understood,[25] and it indicates that this technique is also promising for intercalating thicker Si layers for further practical applications. To date, however, achieving an oxidized Si layer (or an insulating layer) that meets the prerequisite and basis for next generation high-performance electronic devices of graphene, has remained extremely challenging.

In this paper, we demonstrate the fabrication of centimeter-scale, epitaxially grown, single-crystal graphene on an insulating SiO_2 film using a transfer-free process, directly intercalating SiO_2 at the graphene/metal interface. To this end we first prepared a continuous, single-crystal graphene layer on a Ru(0001) surface and then grew silicon dioxide underneath graphene by a

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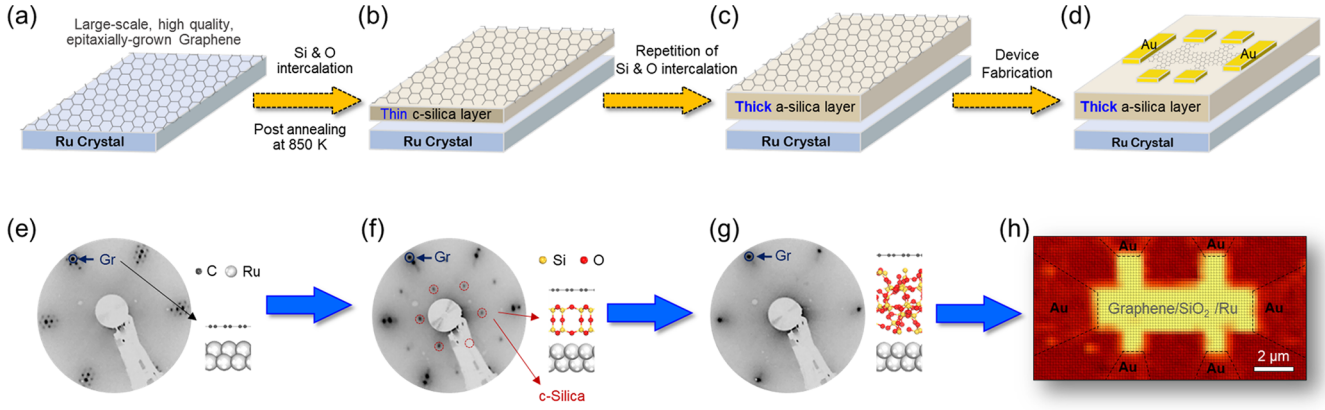

Figure 1. Synthesis of insulating SiO_2 between graphene and a Ru(0001) substrate enabling electronic-device fabrication. (a)−(d) Schematic of sample preparation and device fabrication processes. (a) Large-scale, high-quality graphene layer grown epitaxially on Ru(0001) by exposure to ethylene at 1300 K. (b) Formation of a thin crystalline SiO_2 (c-silica) layer under the graphene by a stepwise intercalation of silicon and oxygen. (c) Formation of a thick amorphous SiO_2 (a-silica) film after repetition of cycles of silicon and oxygen intercalation. (d) Hall-bar device fabrication by using the *in situ* fabricated graphene on thick amorphous SiO_2. (e)−(g) LEED patterns and corresponding structure models for sample in preparation stages (a)−(c), respectively. (e) LEED pattern for sample in (a) shows sharp diffraction spots from graphene and surrounding satellite spots from the Moiré superlattice. (f) Diffraction spots from graphene persist, Moiré spots disappear, and a set of new spots associated with a 2×2 superstructure with respect to Ru(0001) appear, indicating formation of crystalline bilayer silica in stage (b). (g) Except for graphene spots, no extra spot appears, indicating the thick silica in (c) turns amorphous. The intensity of diffraction spots from graphene remains almost unchanged during the whole sample fabrication process. (h) Graphene G-peak intensity mapping, showing the skeleton of the graphene Hall-bar device in (d).

stepwise intercalation of silicon and oxygen at the graphene/Ru interface. Thin crystalline (~1 nm) and thicker (~2 nm) amorphous SiO_2 films are fabricated and confirmed by cross-sectional scanning transmission electron microscopy (STEM) and low-energy electron diffraction (LEED). The topmost epitaxial graphene layer remains high-quality after intercalation and the graphene/SiO_2 interface is smooth. The thick amorphous SiO_2 film serves as a dielectric layer that insulates the graphene from the Ru substrate. Furthermore, the isolated graphene has been used to fabricate Hall bar devices. Low-temperature magneto-transport measurements based on the fabricated devices provide clear evidence of the intrinsic properties of a 2D electron gas in the epitaxial graphene. Shubnikov-de Haas (SdH) oscillations and integer quantum Hall effect show Berry's phase in graphene. Weak antilocalization implies the chirality of the Dirac Fermions. The carrier mobility is measured as ~8500 $cm^2\ V^{-1}\ s^{-1}$, which also confirms the high quality of the graphene on intercalation-grown silicon dioxide. The sample size is controlled by the Ru-substrate size (0.8 cm × 0.8 cm in this case), which is centimeter-scale, having the potential of multiple-device integration.

RESULTS

Procedure of Synthesizing SiO_2 under the Epitaxial Graphene. Panels a−d of Figure 1 illustrate the procedure of fabricating an insulating SiO_2 film between graphene and a Ru substrate and finally the electronic device. First (Figure 1a), a continuous, single-crystal graphene monolayer is epitaxially grown on a clean Ru(0001) substrate.[18,20] At the second stage (Figure 1b), a SiO_2 film is formed underneath the graphene by a stepwise intercalation of silicon and oxygen. We first deposit a moderate amount of silicon on top of graphene and anneal at 900 K, which leads to the intercalation of silicon at the graphene/Ru interface.[23] Afterward, the silicon-intercalated sample is exposed to oxygen at 600 K followed by annealing to 850 K. As a result, oxygen is intercalated underneath the graphene[26] and reacts with the silicon, forming a crystalline silicon dioxide (c-SiO_2) at the interface. At the third stage (Figure 1c), by intercalating additional silicon and oxygen, the silica at the interface becomes thicker and turns amorphous (a-SiO_2). Finally (Figure 1d), *in situ* graphene electronic devices are fabricated by using the thick a-SiO_2 intercalated sample.

LEED and STM Characterizations of the Sample at Each Preparation Stage. The LEED pattern for epitaxial graphene on Ru (Figure 1e), shows sharp diffraction spots from the graphene and surrounding satellite spots from a Moiré superlattice. Continuous LEED patterns on the different regions of the sample remain unchanged (Figure S1), indicating that the graphene layer extends over the entire Ru substrate, i.e., 0.8 cm × 0.8 cm. Both large-scale and atomically resolved scanning tunneling microscopy (STM) images show the defect-free lattice of the as-prepared graphene (Figure S2). The SiO_2 underneath the graphene is formed by silicon intercalation accompanied by subsequent oxidation. After silicon intercalation (900 K), the LEED pattern and STM images (Figure S3) demonstrate that a $\sqrt{7} \times \sqrt{7}$ superstructure with respect to Ru(0001) emerges, suggesting formation of silicene at the graphene/Ru interface.[27] By the subsequent oxygen intercalation (600 K), the underlying silicene is gradually oxidized to be amorphous SiO_2 (Figure S4). Note that the STM images in both Figure S3 and Figure S4 show that the graphene structure remains intact; i.e., the intercalation process does not damage the quality of graphene.[25]

Afterward, the post-intercalation annealing treatment at 850 K converts the amorphous oxide into a crystalline form. As shown in Figure 1f, in addition to the intense spots from graphene, a set of new diffraction spots associated with a 2×2 superstructure with respect to Ru(0001) arises. Such a structure can be assigned to a crystalline SiO_2 bilayer on Ru(0001) surface.[28] We further confirm the schematic structure shown in Figure 1f, using cross-sectional microscopy. Finally, the 2×2 diffraction spots disappear and only the graphene spots remain after additional silicon and oxygen intercalation (Figure 1g), indicating that the thick SiO_2 turns amorphous. The thick a-SiO_2 insulates graphene from the Ru substrate enabling fabrication of

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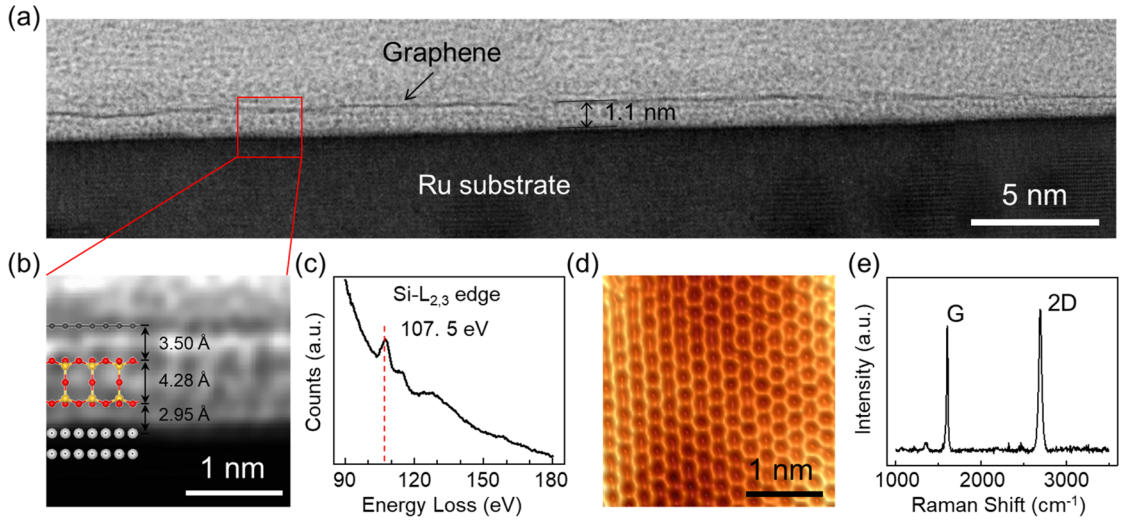

Figure 2. Structure characterizations of the crystalline-bilayer-silica intercalated sample. (a) Large-scale aberration-corrected bright-field STEM image of the bilayer-silica intercalated sample, showing a uniform silica layer with thickness of 1.1 nm under the graphene. (b) High-resolution STEM image taken at the red box in (a) clearly shows the atomic structure of the interfacial silica. The theoretical structure model agrees very well with the experimental results. (c) EELS of Si-$L_{2,3}$ edge taken at the intercalation layer. (d) Atomic-resolution STM image ($V_s = -1.0$ V, $I_t = 500$ pA) showing the intact honeycomb lattice of the graphene overlayer. (e) Raman spectra of the graphene, showing strong G (1604 cm^{-1}) and 2D (2696 cm^{-1}) peaks.

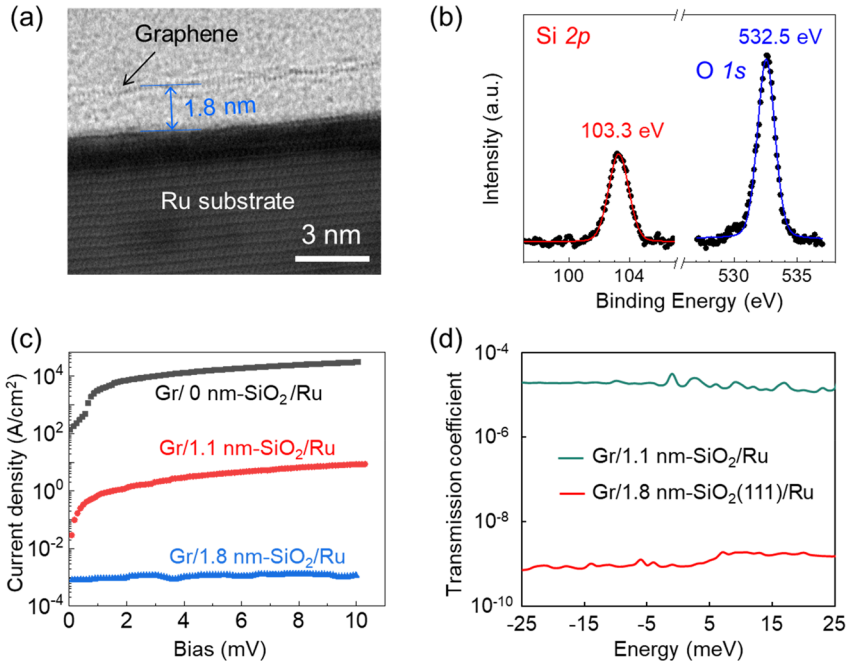

Figure 3. Cross-sectional STEM and vertical transport properties for thick SiO_2 intercalated sample. (a) A STEM image showing a SiO_2 film with thickness of 1.8 nm between graphene and Ru substrate. (b) XPS of the Si 2p and O 1s core levels. (c) Vertical transport measurements at small bias (<10 mV) for Gr/Ru, Gr/1.1 nm-silica/Ru, and Gr/1.8 nm-silica/Ru samples. (d) Calculated transmission coefficient for Gr/1.1 nm-silica/Ru and Gr/1.8 nm-silica/Ru samples.

graphene devices. A Raman map of the graphene G-peak intensity (Figure 1h) clearly shows the graphene channel of a fabricated Hall-bar device.

Structure of Thin Crystalline SiO_2 under the Graphene. We investigated the structures of the underlying SiO_2 with a variety of experimental and theoretical techniques. Figure 2a shows a large-scale STEM image of graphene on crystalline silica. The distance between graphene and the Ru substrate is ~1.1 nm. From the LEED pattern in Figure 1f, the newly appearing 2 × 2 diffraction spots are very sharp and coincide with the pattern of a silica bilayer on Ru(0001) reported previously.[28] The structure of such a silica bilayer on Ru(0001) is composed of corner-sharing [SiO_4] tetrahedra with a lattice constant of about 5.4 Å (twice the lattice constant of Ru(0001)).[28] Considering a graphene layer on top, an atomic structure model for the graphene/c-SiO_2/Ru was established and optimized by using density functional theory (DFT). The top-view and side-view of the optimized structures are shown in Figure S5. Compared with the atomically resolved STEM image in Figure 2b, we find that the theoretical model agrees with the experimental data very well. In Figure 2c, the Si-$L_{2,3}$ EELS shows a peak at 107.5 eV, which is consistent with the Si^{4+} edge in SiO_2,

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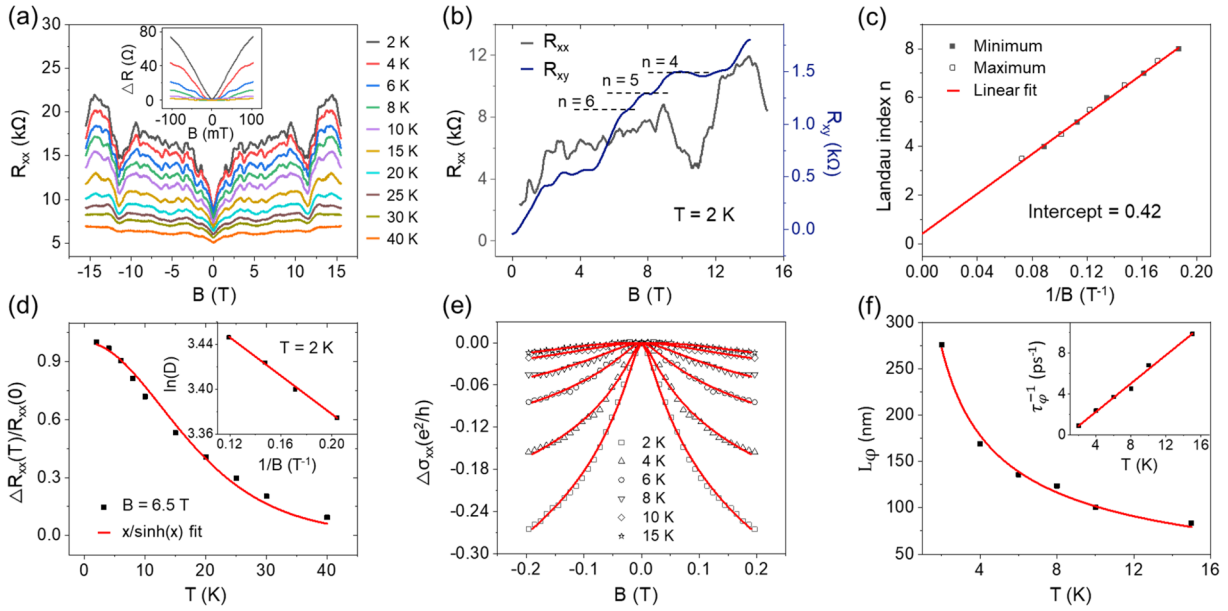

Figure 4. Magneto-transport measurements for the epitaxial graphene. (a) SdH oscillations at different temperatures. For clarity, the curves were shifted vertically. The inset shows low-field magnetoresistance $\Delta R = R_{xx}(B, T) - R_{xx}(0, T)$ at various temperatures. (b) Magnetoresistance R_{xx} (black) and Hall resistance R_{xy} (blue) measured at 2 K. (c) Landau-level fan diagram for SdH oscillations. The location of $1/B$ for the periodic maxima and minima plotted against Landau level index n. The line corresponds to a linear fit, giving an intercept close to 0.5, manifesting a Berry phase of π. (d) Temperature dependence of the normalized amplitude of oscillations. The red solid curve is best fit to the function $x/\sinh(x)$. The inset shows a Dingle plot of $\ln(D)$, $D = (\Delta R/(R_0)\cdot B\cdot\sinh(\lambda(T))$. (e) Corrections of low-field conductivity ($\Delta\sigma_{xx}$) at different temperatures, showing good agreement with the weak antilocalization theory of graphene. (f) Extracted phase coherence length L_ϕ and scattering rate τ_φ^{-1} (inset) as functions of temperature.

further confirming the formation of [SiO_4] tetrahedra at the graphene/Ru interface.[29] The intact honeycomb lattice shown in the STM image (Figure 2d) and the almost absence of the D peak in the Raman spectra (Figure 2e) indicate the high quality of the graphene overlayer. The individual LEED patterns obtained at different positions across the entire sample surface remain almost unchanged, indicating centimeter-scale, single-crystalline graphene on the silica bilayer (Figure S6).

Structure of Thick Amorphous SiO_2 under the Graphene. We now turn to examine further the structure of Figure 1c with the thick amorphous oxide. The cross-sectional STEM image in Figure 3a clearly shows a graphene monolayer and a uniform intercalated film with thickness of ~1.8 nm between the graphene and Ru substrate. X-ray photoelectron spectroscopy (XPS) reveals that the binding energy of the Si 2p and O 1s levels are 103.3 and 532.5 eV (Figure 3b), respectively, indicative of the formation of SiO_2.[24] In addition, the SiO_2 film is amorphous, which agrees with the LEED result in Figure 1g. These results and conclusions are consistent with a previous study that found that more than two layers of silica grown directly on Ru(0001) have an amorphous structure.[30]

Vertical Transport Properties. Our main objective here is to demonstrate that the graphene/a-SiO_2/Ru(0001) structure, whose spatial scale is controlled by the size of the Ru substrate (cm-scale), is suitable for device fabrication; i.e., we have device-quality graphene and insulating oxide. We performed vertical transport measurements to study the insulating effect of the interfacial SiO_2 film. As shown in Figure 3c, vertical transport curves at very low bias voltage (<10 mV) for samples Gr/Ru, Gr/1.1 nm-SiO_2/Ru, and Gr/1.8 nm-SiO_2/Ru are compared. For graphene on Ru without intercalation, we find a very large vertical current density through the graphene/Ru hetero-structure. When a crystalline bilayer silica (1.1 nm) is intercalated at the interface, the vertical transport is reduced by more than 3 orders of magnitude. Finally, the current density is reduced by another 3 orders of magnitude after increasing the thickness of SiO_2 to 1.8 nm. We also performed such vertical transport measurements at different locations on the Gr/1.8 nm-SiO_2/Ru sample. All the measurements show similar results, namely, a very small vertical current density (10^{-4}–10^{-3} A/cm^2) across the Gr/1.8 nm-SiO_2/Ru heterostructure, indicating that the 1.8 nm amorphous SiO_2 film is uniform and is an excellent choice to insulate the graphene from the Ru substrate. To validate the experimental results, we have calculated the transmission coefficient for the samples of Gr/1.1 nm-SiO_2/Ru and Gr/1.8 nm-SiO_2/Ru (Figure S7). The results in Figure 3d show that the transmission coefficient of thick silica (1.8 nm SiO_2) is about 5 orders smaller than that of bilayer silica (1.1 nm), indicating that the 1.8 nm SiO_2 provides a sufficiently large barrier to insulate graphene from Ru.

Measurements on *in Situ* Fabricated Graphene Devices. We established the device quality of the graphene in the structure with the thick, insulating SiO_2 (1.8 nm) intercalated sample, by fabricating graphene devices with Hall-bar geometry and making several key measurements. Figure 4a shows the longitudinal resistance R_{xx} as a function of magnetic field at different temperatures. SdH oscillations are clearly visible and the amplitude of oscillations decays with increasing temperature. In Figure 4b, we plot the magnetic-field-dependent magnetoresistance R_{xx} and the Hall resistance R_{xy} at 2 K. From the Hall slope, the carrier density is determined to be 3.6×10^{12} cm^{-2}. Moreover, R_{xy} exhibits Hall plateaus at the positions of the R_{xx} minima. The device fabrication process we used here involves multiple steps (see Methods in the Supporting Information) and may introduce contamination, which would influence the quality of quantum-Hall-effect measurements. Though contamination cannot be avoided during the complex process, the R_{xy} clearly exhibits Hall plateaus at positions of the

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R_{xx} minima. The quantized values of plateaus are in accordance with $h/(4n + 2)e^2$, where n is the Landau level index. This result strongly indicates the presence of the expected integer quantum Hall effect in the monolayer graphene. The positions of the associated maxima (minima) in R_{xx} against their Landau level index n are plotted in Figure 4c. The intercept of the linear fit to the data with the n-index axis is close to 0.5, providing direct evidence of a Berry phase of π and the presence of Dirac particles.[3] From the SdH oscillations' periodicity we derived a carrier density equal to $\sim 3.9 \times 10^{12}$ cm^{-2}, which is consistent with the value from the Hall measurement.

The temperature-dependent amplitude of the SdH oscillations at a fixed magnetic field can be described by $\Delta R(T)/R(0) = \lambda(T)/\sinh(\lambda(T))$, where $\lambda(T) = (2\pi^2 k_B T m_c)/\hbar e B$, m_c is the cyclotron mass, $\hbar$ is the reduced Planck's constant, and k_B is Boltzmann's constant. By performing the best fit of the oscillation amplitude to the equation, m_c is extracted to be $\sim 0.06 m_e$ (m_e is the free electron mass), as shown in Figure 4d. In addition, the transport lifetime τ can be estimated utilizing a Dingle plot since $\Delta R(B)/R(0) \sim [\lambda(T)/\sinh(\lambda(T))]\cdot\exp(-\pi m_c)/eB\tau)$. As shown in the inset of Figure 4d, the transport lifetime is estimated to be 3×10^{-13} s. The carrier mobility $\mu = e\tau/m_c$ is estimated as 8500 cm^{-2} V^{-1} s^{-1}, which is larger than that of directly grown graphene on dielectrics.[13−15]

Low-field magnetoresistance is a sensitive probe for electronic transport as it measures the effect of quantum interference. In particular, 2D electron systems in the presence of low magnetic field show corrections to the resistance induced by quantum interference, which is known as a weak (anti-)localization effect. Here, we observed a broad cusplike depression in the longitudinal resistance R_{xx} in the low-magnetic-field regime (Figure 4a), implying a weak antilocalization characteristic in the epitaxial graphene.[31,32] The temperature-dependent magnetoconductance $\Delta\sigma_{xx}$ is shown in Figure 4e. The cusps are broadened and finally disappear as the temperature increases.

Considering the inelastic scattering, elastic (phase breaking) intervalley and intravalley scattering, the corrections to the magnetoconductance are well fitted by the expression[32,33]

$$\Delta\sigma(B) = \frac{e^2}{\pi h}\left\{F\left(\frac{\tau_B^{-1}}{\tau_\varphi^{-1}}\right) - F\left(\frac{\tau_B^{-1}}{\tau_\varphi^{-1}+2\tau_i^{-1}}\right) - 2F\left(\frac{\tau_B^{-1}}{\tau_\varphi^{-1}+\tau_i^{-1}+\tau_*^{-1}}\right)\right\}$$

where $F(z) = \ln(z) + \psi(0.5 + z^{-1})$, $\tau_B^{-1} = 4eDB/\hbar$, ψ is the digamma function, and D is the diffusion coefficient. By using the relation $L_{\varphi,i,*} = \sqrt{D\cdot\tau_{\varphi,i,*}}$, we can extract the corresponding scattering length. The obtained coherence length L_φ and corresponding scattering rate τ_φ^{-1} as a function of temperature are shown in Figure 4f. The power law dependence of the coherence length $L_\varphi \sim T^{-1/2}$ and linear dependence of scattering rate τ_φ^{-1} indicate that the dominant phase-breaking mechanism is electron−electron scattering, which is consistent with previous studies.[32] The weak antilocalization effect implies the chiral electronic character in the epitaxial graphene and further confirms the presence of a Berry phase of π.[32] Additionally, the observation of such phenomena is attributed to the suppression of point defects, suggesting high quality of the epitaxially grown graphene on the silicon dioxide film.

DISCUSSION

The vertical transport measurements on Gr/Ru, Gr/1.1 nm-SiO_2/Ru, and Gr/1.8 nm-SiO_2/Ru show that the current density has been reduced by 6 orders of magnitude when the thickness of SiO_2 reaches 1.8 nm. Further magneto-transport measurements on the *in situ* fabricated Hall-bar devices using Gr/1.8 nm-SiO_2/Ru show intrinsic electronic properties from graphene, indicating that the intercalation of SiO_2 layer with 1.8 nm in thickness keeps graphene intact and insulates the graphene from Ru completely. This *in situ* sample growth and device fabrication process provides a straightforward avenue to utilize the large-scale, high-quality graphene grown on a metal substrate. The 1.8 nm amorphous SiO_2 is enough to insulate graphene from Ru substrate; however, to make a field-effect transistor that can be used in future electronics, intercalation of a thicker, uniform SiO_2 layer is needed.

In this work, we chose Ru(0001) as the growth substrate because the graphene layer epitaxially grown on Ru(0001) is high quality and single crystalline and has continuity in the large scale. The SiO_2 intercalation technique can be used on Ru substrates of different sizes. For instance, intercalation of crystalline SiO_2 below graphene has been realized on Ru substrates in the three sizes, 0.4 cm × 0.4 cm, 0.8 cm × 0.8 cm, and 1 cm diameter, as shown in Figure S8. As an alternative to single-crystal Ru substrates, which are expensive, we note that graphene grown on Ru thin films and grown on SiO_2/Si or sapphire substrates is comparable in quality to that grown on single-crystal Ru.[34,35] Thus, for consideration of commercial scale-up, the transfer-free technique can be extended to graphene/Ru thin film systems. This technique can be applied not only to Gr/Ru but also to graphene grown on other metal substrates, for example, Ni, Ir, Cu, and Pt. Moreover, it can be utilized to insulate graphene nanoribbons or other 2D materials from their metal supports, providing a route to electronic-device fabrication and applications based on 2D materials.

CONCLUSIONS

We have successfully integrated centimeter-scale, high-quality graphene on an insulating SiO_2 film by using a transfer-free approach, directly intercalating SiO_2 at the interface between epitaxial graphene and a metal substrate. By LEED and cross-sectional STEM characterizations, we find that thin crystalline and thicker amorphous SiO_2 films can be grown under the graphene overlayer, while the graphene/SiO_2 interface stays clean and sharp. STM and Raman measurements confirm that the epitaxial graphene remains high-quality after the intercalation process. Eventually, a pure SiO_2 film with a thickness of 1.8 nm successfully insulates graphene from the Ru substrate, which enables the fabrication of a graphene-based device. By magneto-transport measurements on *in situ* fabricated Hall-bar devices, the intrinsic properties of 2D electron gas in the high-quality epitaxial graphene are clearly observed, confirming that the intercalation of SiO_2 layer keeps graphene intact and insulates graphene from Ru completely. The present work provides a reliable platform to realize potential applications of graphene in electronics and paves the way to directly synthesize large-scale, high-quality graphene on insulating substrates.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.0c03254.

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More details for the sample preparation, measurement systems, fabrication procedures of *in situ* graphene devices, and transport calculation methods, and Figures S1−S9 of LEED measurements, STM images, structure models, photos of Ru substrates, and fabrication procedures (PDF)

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Author Contributions

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Author Contributions

H.G., X.Y.W., L.H., and L.H.B. performed the LEED, STM, Raman, and XPS measurements and fabricated the transistors. H.G. and Z.Z. performed the transport measurements. Z.Z.Y., Q.H.Z., and L.G. performed the STEM measurements. X.J., Y.Y.Z., S.X.D., and S.T.P. carried out the theoretical calculations. H.G., L.H., H.H., Y.Y.Z., H.L.L. C.M.S., X.L., Q.D., L.H.B., S.X.D, W. H., S.T.P., and H.J.G. analyzed the data and wrote the manuscript. All authors discussed and commented on the work. H.J.G, S.X.D, and L.H.B. designed and coordinated the project.

Notes

The authors declare no competing financial interest.

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